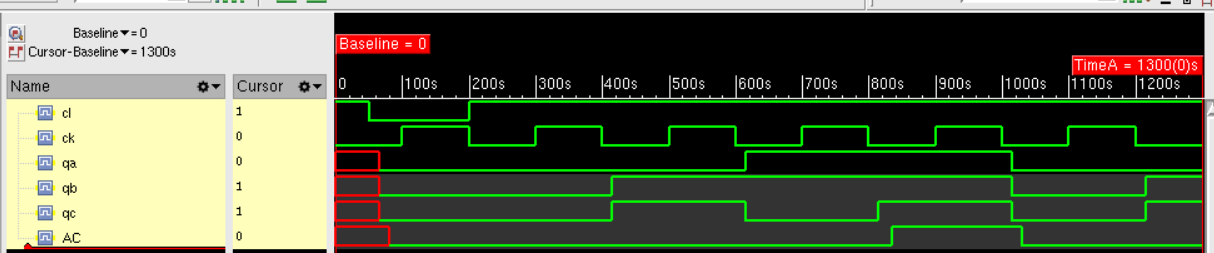
Hw set 9 Victor Yuan

1. 

Code for it:

module test;

reg cl,ck; // inputs

parameter high=1'b1; // logic 1

jkff\_74LS107A

U1A(qb,qc,cl,ck,qa,qabar),

U1B(high,AC,cl,ck,qb,qbbar),

U2A(high,high,cl,ck,qc,qcbar);

and #(20,15) U3A (AC,qc,qa);

initial ck=0;

always #100 ck=~ck;

initial

begin

$monitor($time,"cl=%b ck=%b qa=%b qb=%b qc=%b AC=%b", cl,ck,qa,qb,qc,AC);

#000 cl=1;

#050 cl=0;

#150 cl=1;

#1100 $finish;

end

endmodule

module jkff\_74LS107A(j,k,cl,ck,q,qbar);

input j,k,cl,ck; // inputs

output q,qbar; // outputs

parameter delay\_rise=15; // rise time delay

parameter delay\_fall=15; // fall time delay

supply1 pr; // constant logic 1 value

and #(0) (and1,qqbar,nand2,pr),

(and2,qqbar,ck,pr),

(and3,qq,nand1,cl),

(and4,qq,ck,cl);

nand #(1) (nand1,pr,qq,k,ck),

(nand2,cl,qqbar,j,ck);

nor #(0) (qq,and1,and2),

(qqbar,and3,and4);

buf #(delay\_rise,delay\_fall)

(q,qq),

(qbar,qqbar);

endmodule

2.



module main;

reg cl,ck; // inputs

wire qa,qb,qc; // outputs

parameter high=1'b1; // logic 1

dff\_7474

U1A(qb,cl,high,ck,qa,qabar),

U1B(AB,cl,high,ck,qb,qbbar),

U2A(qcbar,cl,high,ck,qc,qcbar)

;

and #(17.5,12) U3A(AA,qc,qb);

or #(10,14) U4A(AB,AA,qabar);

initial ck=0;

always #100 ck=~ck;

initial

begin

$monitor($time,,"cl=%b ck=%b qa=%b qb=%b qc=%b", cl,ck,qa,qb,qc);

#000 cl=1;

#050 cl=0;

#150 cl=1;

#1100 $finish;

end

endmodule

module dff\_7474(d,cl,pr,ck,q,qbar);

input d,cl,pr,ck; // inputs

output q,qbar; // outputs

parameter delay\_rise=14; // rise time delay

parameter delay\_fall=20; // fall time delay

nand #(0) (qq,pr,nand2,qqbar),

(qqbar,qq,cl,nand3),

(nand1,pr,nand4,nand2),

(nand2,nand1,cl,ck),

(nand3,nand2,ck,nand4),

(nand4,nand3,cl,d);

buf #(delay\_rise,delay\_fall)

(q,qq),

(qbar,qqbar);

endmodule